

Method and system using hardware assistance for instruction tracing
with secondary set of interruption resources

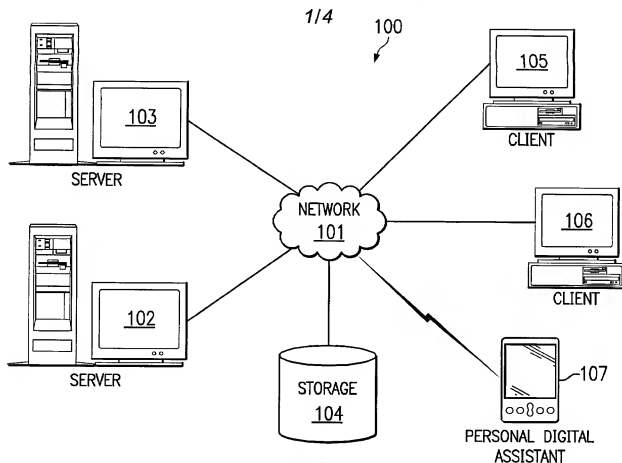


FIG. 1A
(PRIOR ART)

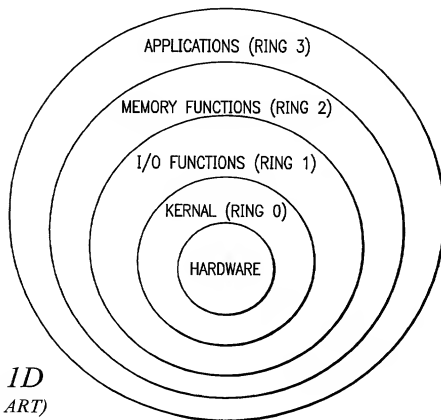


FIG. 1D
(PRIOR ART)

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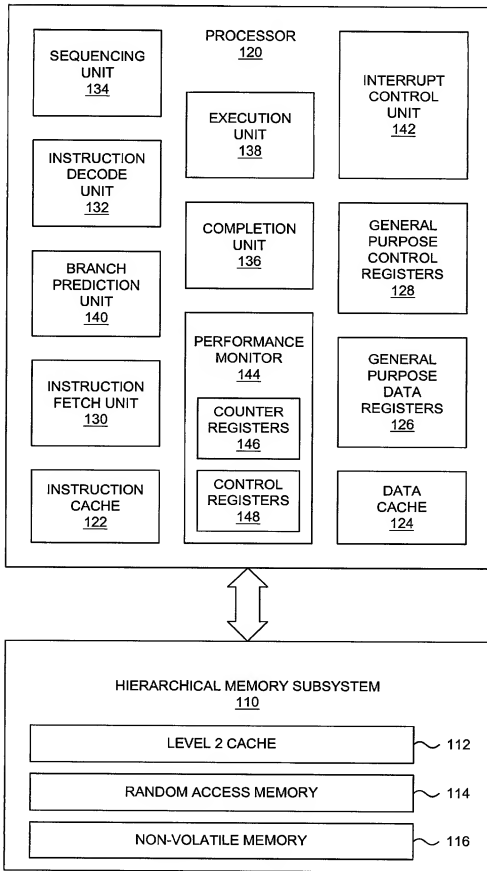


FIG. 1B
(PRIOR ART)

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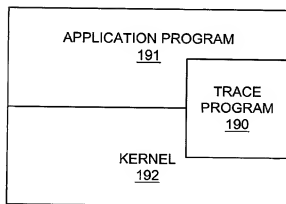


FIG. 1E
(PRIOR ART)

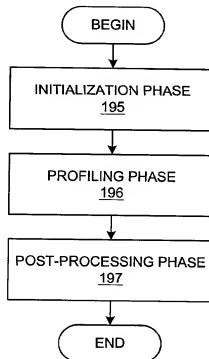


FIG. 1F
(PRIOR ART)

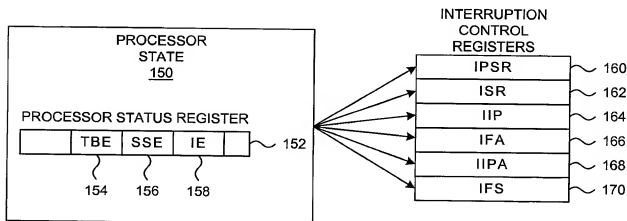


FIG. 1C
(PRIOR ART)

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FIG. 2A

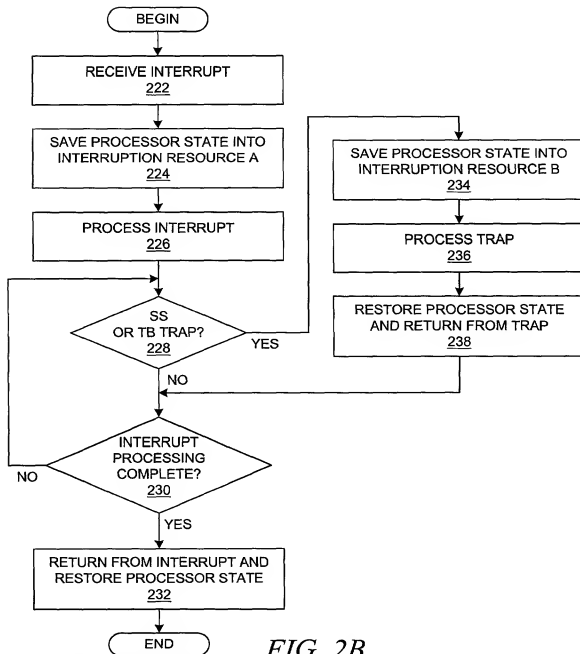
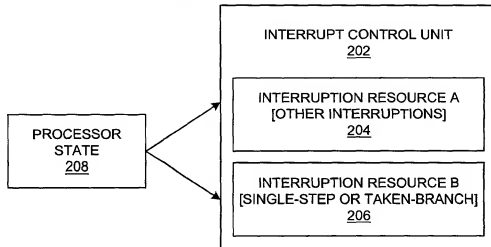


FIG. 2B